

Description

Electronic component and method for producing it

5 The invention relates to an electronic component with a semiconductor substrate for a micro-electromechanical system, an active top side on the semiconductor substrate having an active surface area which is covered by a self-supporting electrically conductive
10 covering element. Furthermore, the invention relates to a semiconductor wafer having a number of such components and to a method for producing such an electronic component or semiconductor wafer, respectively.

15 The increasing miniaturization, particularly in micro-electromagnetic and micro-electromechanical systems, also called MEMS, requires covering, shielding and/or resonant structures of electrically conductive
20 materials, the structure of which is complex and the assembly of which requires elaborate tools which, at the same time, sets limits to the degree of miniaturization for covering, shielding and/or resonant structures.

25 The assembly, in which each covering, shielding and/or resonant element must be attached individually to a semiconductor substrate, is also cost-intensive.

30 It is the object of the invention to specify an electronic component which increases the degree of miniaturization in covering, shielding and/or resonant structures and which can be produced inexpensively.

35 This object is achieved by means of the subject matter of the independent claims. Advantageous developments of the invention are obtained from the dependent claims.

The electronic component according to the invention comprises a semiconductor chip with a semiconductor substrate. On the semiconductor substrate, an active top side is arranged. On the active top side, an active surface area is located. This active surface area is a part of a micro-electromechanical system. This active surface area is connected to contact connecting areas on the active top side of the semiconductor substrate.

10 The package of the electric component comprises a package-forming plastic layer which covers the substrate, leaving the contact connecting areas exposed. Between the package-forming plastic layer and the active top side of the semiconductor substrate, a self-supporting electrically conductive cover layer is arranged above the active surface area. This cover layer is supported by through lines to the active top side and forms a hollow space which extends between the active surface area and cover layer.

20 The height of the hollow space corresponds to a thickness of an insulation layer, metal layer or photoresist layer, which is normal for semiconductor wafers and which can be applied as sacrificial layer on a semiconductor wafer. The hollow space can thus comprise a height in the submicrometer range up to a few micrometers. In this context, the submicrometer range means a thickness between 100 nm and 1 μm . A few micrometers means a thickness between 1 μm and approx. 20 μm .

Due to the low height of the hollow space, not only is the degree of miniaturization of microelectromechanical systems increased but the interaction between the cover and the active components, arranged underneath it, of the active surface area is intensified. This makes it possible to produce more effective microphones and more effective fine-line patterned effectors. In addition, more sensitive sensors and filters with sharper cut-off

can be implemented from microelectromechanical structures.

5 In addition, the electronic component according to the invention makes it possible to achieve a very flat and small type of construction which makes it possible to integrate such components into modules for frequency filter systems in the mobile telephone field, particularly with structure-borne waveguides or with
10 surface acoustic waveguides. To supply and remove signals to the active surface area and for applying supply voltages to the self-supporting electrically conductive cover layer, the electronic component has contact connecting areas which are connected both to
15 the active surface area and to the cover layer via conductor tracks, the contact connecting areas in a first embodiment of the invention carrying external contacts of the electronic component.

20 Furthermore, the package-forming plastic layer, leaving the contact connecting areas or the external contacts, respectively, exposed, can cover the cover layer in such a manner that the hollow space underneath the cover layer is laterally sealed between the
25 load-bearing through lines. This results in a hermetically sealed hollow space which, after being covered by the package-forming plastic layer, is subjected to a reference pressure.

30 To hold the self-supporting cover layer at a minimum distance above the active surface area, the load-bearing through lines are arranged regularly distributed around the circumference of the cover layer. Such through lines can carry cover layers of
35 several 100 μm edge length and are distributed at an interval of 10 to 50 μm around the circumference of the cover layer.

As electrically conductive material, the cover layer comprises a metal or a semiconductor material. For this purpose, the semiconductor material is heavily doped. The semiconductor material used is preferably
5 polycrystalline silicon with a dopant concentration of more than $10^{19}/\text{cm}^3$. The metal of the cover layer is nickel, copper, aluminum or alloys thereof, silicon being used as alloying addition in order to increase the stiffness of the metals.

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The electronic components according to the invention can be arranged in rows and columns on semiconductor wafers which has the advantage that all components of the electronic components from the external contacts to
15 the self-supporting cover layers can be provided in parallel and at the same time on the semiconductor wafer. A further aspect of the invention relates to a use in which the electronic components are arranged in rows and columns with microelectromechanical patterns.
20 The use differs from the semiconductor wafer in that the semiconductor chips are arranged in a plastic compound or on a corresponding circuit board distributed at a predetermined distance on a larger area than in the case of the semiconductor wafer. The
25 advantage of such a use consists in that the size and number of external contacts can be arbitrarily increased since between the semiconductor chips, larger plastic areas or larger circuit board surfaces are available for arranging the external contacts of the
30 electronic components.

A method according to the invention for producing a semiconductor wafer with a number of semiconductor chips for a number of electronic components has the
35 following method steps. Firstly, a semiconductor wafer having a number of semiconductor chip positions arranged in rows and columns is provided. Then active surface areas are created on the active top side of the semiconductor wafer in the semiconductor chip positions

and outside these active surface areas, contact areas are applied to the active top side of the semiconductor wafer. Following this, a sacrificial layer is applied and patterned. After the patterning, the sacrificial layer covers the active surface area and comprises through openings in the edge areas of the active surface area which extend to the active top side of the semiconductor substrate in the form of a semiconductor wafer.

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As the sacrificial layer, oxides, nitrides or photoresists can be applied and patterned. Following this, a conductive material which, at the same time, forms through lines, connected to the cover layer, in the through openings, is applied to the sacrificial layer. These through lines are distributed around the circumference of the cover layer. This makes it possible to remove the sacrificial layer between the through lines and under the cover layer. During this process, a cover layer which is supported by through lines and is self-supporting is created above the active surface area, forming a flat hollow space.

Next, a plastic layer is applied as packaging to the cover layer and the active top side, leaving the contact connecting areas exposed. At the same time, this first plastic layer seals the side edges of the hollow space and thus closes the gaps between the supporting and load-bearing through lines. Since, when the first plastic layer is applied or the first plastic layer is patterned thereafter, the contact connecting areas are left exposed, external contacts for the electronic components can already be applied to the contact connecting areas on the whole semiconductor wafer. Thus, these external contacts are applied simultaneously on one and the same semiconductor wafer for many electronic components. Thereafter, the semiconductor wafer can be split into individual electronic components.

This method has the advantage that covering, shielding and/or resonant structures for individual electronic components do not need to be assembled and produced separately and individually but that they can be implemented in parallel on a semiconductor wafer. In addition, the method has the advantage that the dimensions of such covering, shielding and/or resonant structures can reach a higher degree of miniaturization as a result of which, on the one hand, higher operating frequencies and, on the other hand, greater interactions between covering, shielding and/or resonant layer and active surface areas arranged underneath in a hollow space can be achieved.

The patterned sacrificial layer applied in the method can be deposited on the semiconductor wafer from a chemical gas phase, forming silicon oxide or silicon nitride. Another variant consists in applying a sacrificial metal layer, the etching rate of which differs significantly from an etching rate of the patterned conductive cover layer applied so that the sacrificial layer can be etched out more rapidly than the cover layer is removed. For this purpose, reactive plasma etching methods are used. Another possibility of forming a sacrificial layer consists in applying a photoresist layer on the semiconductor wafer by spinning or spraying it on and patterning it with the aid of photolithography.

The material of the sacrificial layer essentially depends on the possibilities of deposition and application for the self-supporting electrically conductive cover layer. If a polycrystalline silicon is deposited from an organometallic compound in the chemical gas phase method, a sacrificial layer of silicon oxide or silicon nitride is preferably provided which can be removed subsequently by means of hydrofluoric acid in the case of the silicon oxide.

When a metallic cover layer of preferably nickel, copper, aluminum or alloys thereof is applied, a photoresist can be applied to the semiconductor wafer. A sacrificial layer of photoresist can be subsequently
5 removed by means of solvents which protects the surfaces of the active surface area and the metallic cover layers. A cover layer of nickel or nickel alloys enables a sacrificial layer of copper or of a copper alloy to be used since copper etchants can be used
10 which have a negligible effect on the cover layer of nickel or nickel alloys.

In a further variant of the performance of the method according to the invention, a rewiring pattern is then
15 applied to the first plastic layer for sealing the side edges of the cover layer and for packaging the active surface of the semiconductor wafer. The rewiring pattern and the first plastic layer are covered with a second plastic layer as package-forming layer, leaving
20 the external contact areas exposed.

The rewiring pattern on the first plastic layer is used for connecting the contact connecting areas via rewiring lines to correspondingly larger external
25 contact areas on the first plastic layer or prepared through openings in the first plastic layer. The second plastic layer then covers the entire first plastic layer with the rewiring pattern and only leaves an access to the external contact areas exposed. Thus,
30 external contacts can be applied to the external contact areas for the entire semiconductor wafer. Both the first plastic layer and the second plastic layer can consist of epoxy resin. However, it is advantageous to use as the second plastic layer polyamide which, at
35 the same time, is used as solder resist layer for applying the external contacts.

In summary, it must be noted that the cavity package according to the invention is distinguished by the fact

that all processes for generating the semiconductor chip, the hollow space, the electric rewiring and the electric contacting can already be performed at wafer level. Thus, this is a so-called "wafer level package",
5 which can be achieved with very small constructional size for the abovementioned applications which need a hollow space above an active chip area. The method for producing microelectromechanical structures requiring such a hollow space lies in the fact that no
10 multi-layer substrate is required for rewiring and no back-end process is needed for creating the hollow space.

By means of the introduction of a micromachining
15 process for creating the hollow space at wafer level, etching out a sacrificial layer and sealing remaining openings by applying an additional polymer layer, it is possible to combine this structure with electrical contacts, also at wafer level. In addition, it is also
20 possible to implement a rewiring plane at wafer level so that the abovementioned advantages such as small component size, microscopically small hollow spaces above active areas and possibilities for adapting external contact areas via rewiring planes to
25 predetermined package sizes are possible. At the same time, processing at wafer level results in low production costs.

The inexpensive possibility exists to implement the
30 first plastic layer for sealing the sides of the hollow spaces by applying polymer foils or by laminating and spraying-on polymer layers. Applying external contacts can be done by applying solder balls. In addition, it is possible to arrange rewiring lines on the first
35 plastic layer above the area of the cover layer or the lid of the hollow space since the first plastic layer can be used at the same time as insulator for the rewiring lines.

The invention will now be explained in greater detail with reference to the attached figures.

5 figure 1 shows a diagrammatic cross section through an electronic component of a first embodiment of the invention,

10 figure 2 shows a diagrammatic cross section through a semiconductor wafer in the area of an active surface area to be covered, with a patterned sacrificial layer,

15 figure 3 shows a diagrammatic cross section through a semiconductor wafer according to figure 2 after a patterned electrically conductive cover layer has been applied to the sacrificial layer,

20 figure 4 shows a diagrammatic cross section through a semiconductor wafer according to figure 3, after the sacrificial layer has been removed,

25 figure 5 shows a diagrammatic perspective view of a section of a semiconductor wafer with a cover on an active surface area,

30 figure 6 shows a diagrammatic cross section through an electronic component of a second embodiment of the invention.

35 Figure 1 shows a diagrammatic cross section through an electronic component 1 of a first embodiment of the invention. The electronic component 1 has a semiconductor chip 2 with a semiconductor substrate 3 on which an active top side 4 with an active surface area 5 is arranged. On the active top side 4, outside the active surface area 5, contact connecting areas 6 are arranged which are electrically connected to the active surface area 5 via conductor tracks, not shown.

A package 7 comprises a package-forming plastic layer 8 which covers the active top side 4 of the semiconductor chip 2. The remaining outsides of the electronic component 1 are formed by outside surfaces 19 of the semiconductor substrate in the first embodiment according to figure 1. The package-forming plastic layer 8 does not cover the contact connecting areas 6 on which external contacts 14 are arranged according to figure 1. Above the active surface area 4 of the semiconductor substrate 3, a self-supporting electrically conductive cover layer 9 is arranged.

The cover layer 9 forms a protecting, shielding or resonance structure for the active surface area 5 arranged on the active top side 4. The self-supporting cover layer 9 is connected to through lines 10 which extend to the active top side 4. Between the active surface area 5 and the cover layer 9, a hollow space 11 extends, the height h of which corresponds to the thickness of an insulating layer, a metal layer or a photoresist layer on a semiconductor wafer, in this case within the range of between $0.3\text{ }\mu\text{m}$ and $3\text{ }\mu\text{m}$. Larger hollow spaces, not shown here, having a height of up to $20\text{ }\mu\text{m}$ are achieved by means of thicker sacrificial layers such as an electroplated copper layer. The self-supporting cover layer 9 has a thickness which corresponds to a thickness of conductor tracks on a semiconductor wafer or on a circuit board, approximately within the range of from 0.3 to $10\text{ }\mu\text{m}$.

To produce such an electronic component 1, a semiconductor wafer having a number of semiconductor chip positions arranged in rows and columns is first provided. A section of such a semiconductor wafer 13 can be seen in figure 2.

Figure 2 shows a diagrammatic cross section through a semiconductor wafer 13 in the area of an active surface

area 5, which is to be covered, with a patterned sacrificial layer 21. In figure 2, the generation of an active surface area 5 for a MEM (micro-electromechanical) structure is thus already concluded
5 and a patterned sacrificial layer 21 is applied above the active surface area 5. This patterned sacrificial layer 21 on the active top side 4 of the semiconductor wafer 13 has through openings 22 in the edge area of the active surface area 5. The sacrificial layer 21
10 itself is a silicon dioxide layer with a thickness of 1.2 μm in this exemplary embodiment of the method according to the invention. The edge length l of the active surface area 5 is approx. 75 μm and the width b of the openings 22 is approx. 15 μm in this embodiment
15 of the invention.

Figure 3 shows the semiconductor wafer 13 according to figure 2 after a patterned electrically conductive cover layer 9 has been applied to the sacrificial layer
20 21. The cover layer 9 also fills up the openings 22 in the sacrificial layer 21 so that the through lines 10 produced in the through openings 22 will later support the cover layer 9. In this example of performance of the method, the cover layer 9 was formed in an
25 organometallic gas phase reactor in which a heavily doped polycrystalline silicon with a thickness of between 0.3 and 10 μm is deposited on the sacrificial layer 21 and in the openings 22. After the patterning of the deposited polycrystalline silicon layer, the
30 diagrammatic cross section according to figure 3 is obtained.

Figure 4 shows the semiconductor wafer 13 according to figure 3 after removal of the sacrificial layer 21. The
35 sacrificial layer of silicon oxide is removed by means of buffered hydrofluoric acid which does not attack the heavily doped polycrystalline silicon. After the sacrificial layer has been etched out, the self-supporting metallically conductive cover layer 9

remains above the active surface area 5 on the active top side 4 of the semiconductor wafer 13, forming a hollow space 11.

5 Between the filled-up openings 22 according to figure 3, gaps 25 are produced during the etching through which the hydrofluoric acid can also penetrate below the cover layer 9. Due to the high affinity of the hydrofluoric acid to silicon dioxide, the entire
10 silicon dioxide layer can be etched off under the cover 9 of polycrystalline silicon. In addition, the dimensional stability and stiffness of the polycrystalline silicon ensures that the cover layer 9 becomes a cover which is supported in a self-supporting
15 manner on the lateral through lines 10. Due to the gaps 25 between the through lines 10, the hollow space 11 produced is not hermetically sealed and not protected against environmental influences. This protection is achieved by a first plastic layer, not shown here,
20 which is subsequently deposited.

Figure 5 shows a diagrammatic perspective view of a section of the semiconductor wafer 13 from figure 4. The cover 24 is self-supporting and covers the active
25 surface area 5 by forming a hollow space 11. The self-supporting cover 24 is supported to the top and to the side by the through lines 10 which are of the same material as the cover 24. Between the supports in the form of through lines 10, the gaps 25 are arranged.

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Figure 6 shows a diagrammatic cross section through an electronic component 100 according to a second embodiment of the invention. Components having the same functions as in figure 1 are identified by the same
35 reference symbols and are not separately explained.

A difference between the first embodiment according to figure 1 and the second embodiment according to figure 6 consists in that enlarged external contact areas 18

are arranged next to contact connecting areas 6 on the active top side 4 of the semiconductor chip 2. Whereas the contact areas 6 are connected to the active surface area 5 via conductor tracks, not shown here, the external contact areas 18 carry additional enlarged external contacts 14. For this purpose, a rewiring pattern 16 with rewiring lines 17 is applied to the first plastic layer 15, the rewiring lines 17 electrically connecting the contact connecting areas 6 to the external contact areas 18. As protection, and to insulate the rewiring pattern 17, a further second package-forming plastic layer 20 is applied to the first plastic layer 15, leaving the external contact areas 18 exposed.

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In the cross section according to figure 6, it cannot be seen that the rewiring lines 16 extend on the first plastic layer 15. As a result, the insulated surface produced in the area of the cover is utilized for the wiring. The external contacts 14 themselves here have the form of solder balls. The second plastic layer 20 is simultaneously used as solder resist layer when the external contacts 14 are soldered to the external contact areas 18.

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